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(54) **ORGANIC LIGHT EMITTING DIODE DISPLAY**

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(57) **ABSTRACT**

An organic light emitting diode display includes: a substrate including a display area and a non-display area adjacent to the display area; a pixel thin film transistor positioned in the display area of the substrate; a first data wire positioned on the pixel thin film transistor; a second data wire positioned on the first data wire; an organic light emitting element positioned on the second data wire and electrically connected to the pixel thin film transistor through the first data wire and the second data wire; a circuit unit positioned in the non-display area of the substrate and including a circuit thin film transistor electrically connected to the pixel thin film transistor; and a common power supply line overlapping at least part of the circuit unit, electrically connected to the organic light emitting element, and formed on a same layer as the second data wire.

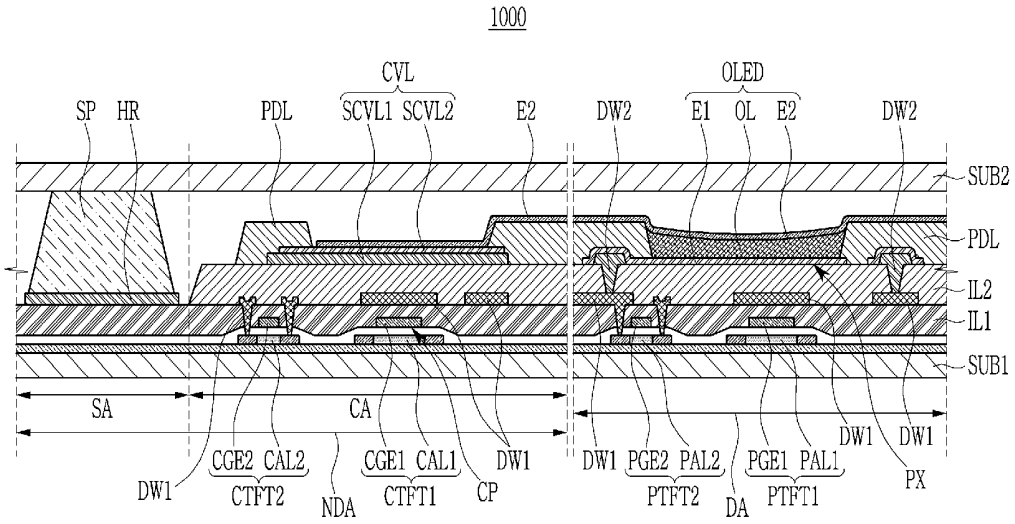


FIG. 1

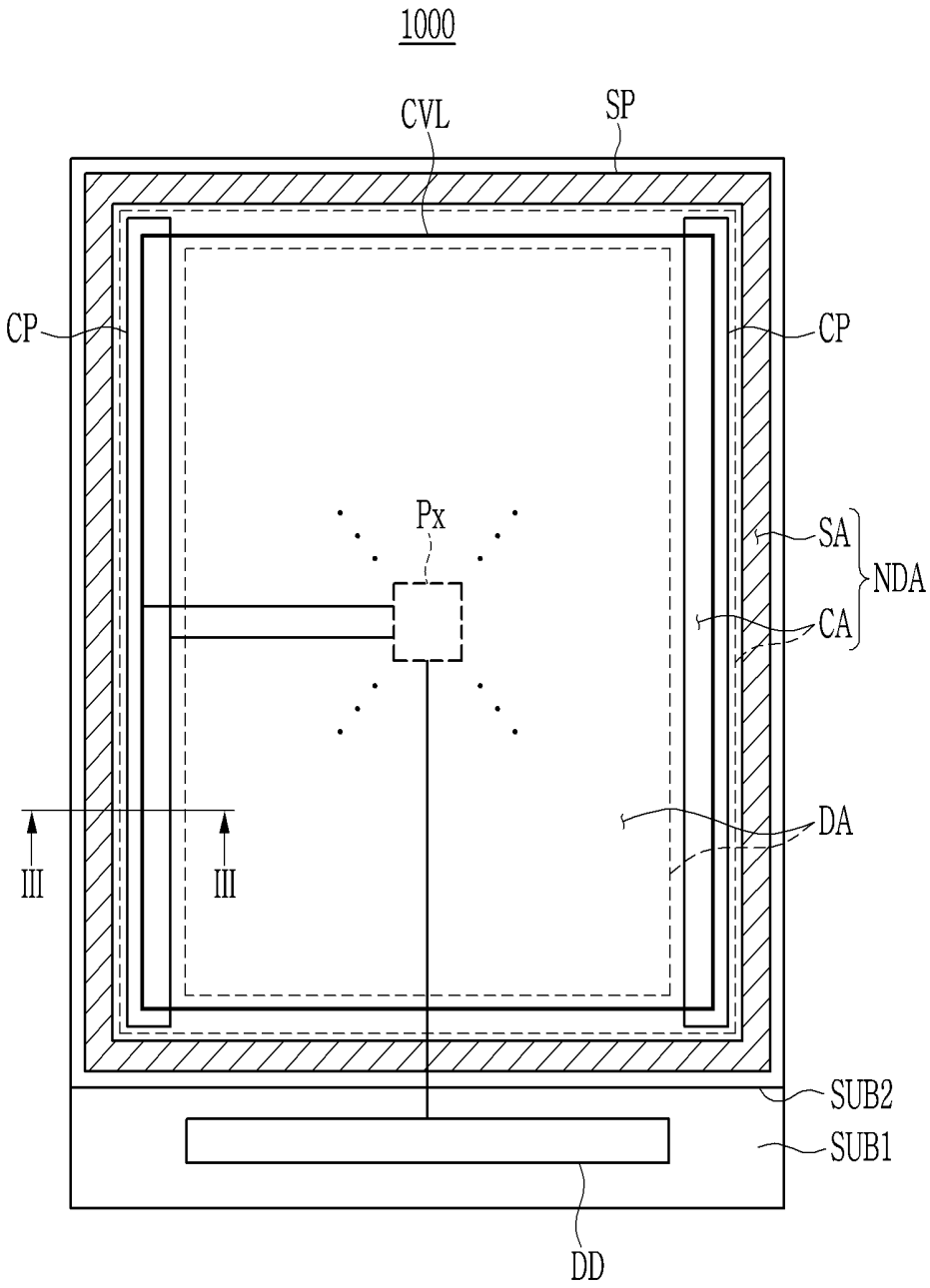


FIG. 2

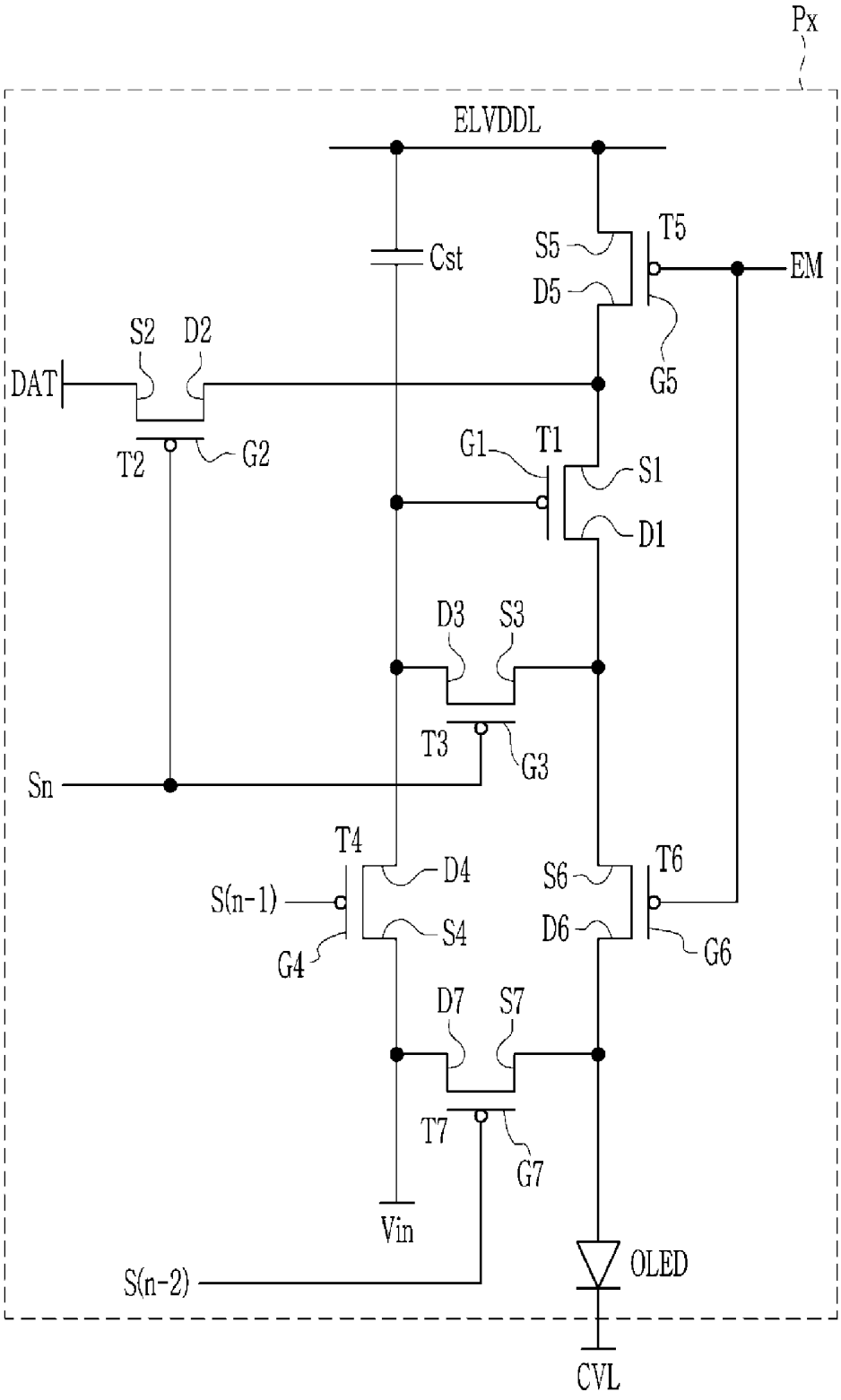

Px
ELVDDL
Cst
S5
T5
EM
D5
S2
D2
DAT
G5
T2
G2
G1
T1
S1
D1
D3
S3
T3
G3
Sn
T4
D4
S6
T6
S(n-1)
S4
D6
G4
G6
D7
S7
T7
G7
Vin
OLED
S(n-2)
CVL

FIG. 3

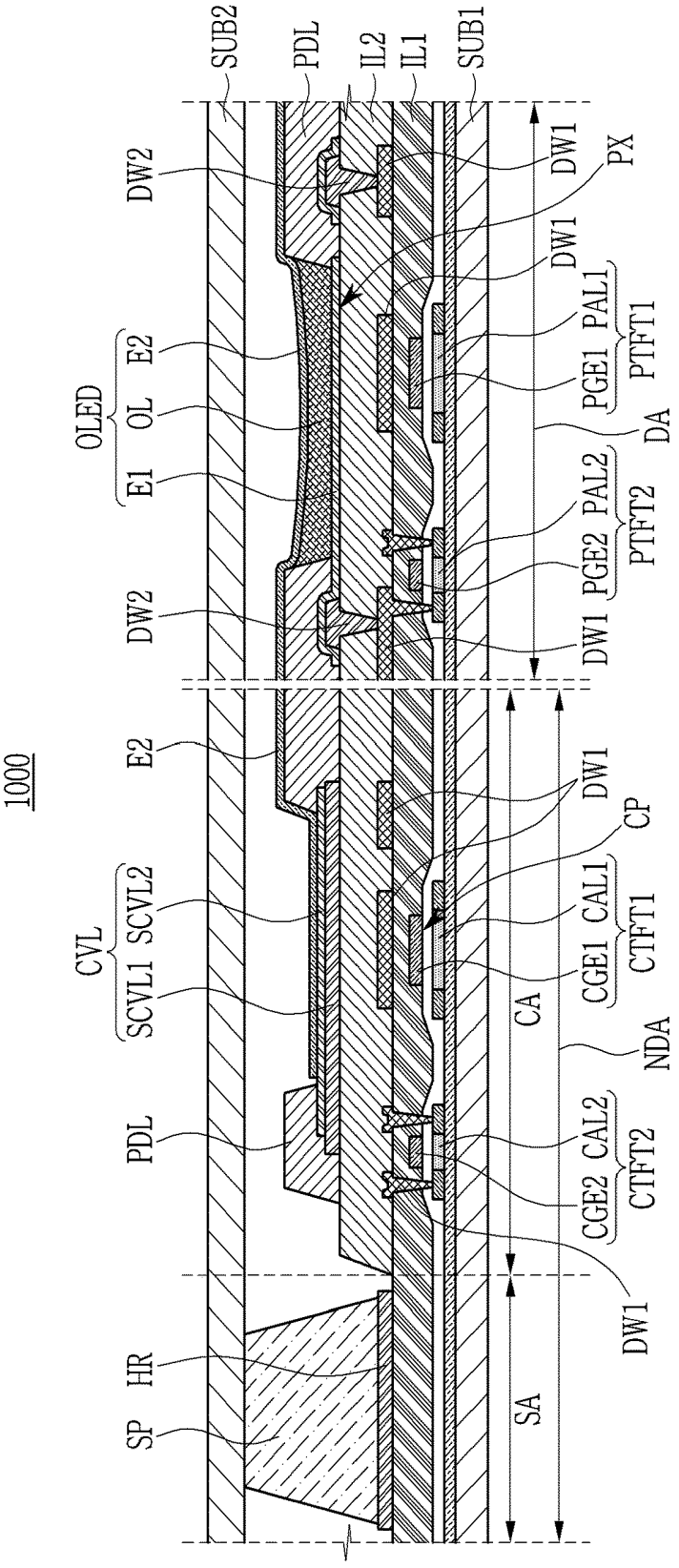

1000
SUB2
PDL
IL2
IL1
SUB1
DW2
DW1
PX
OLED
E2
OL
E1
PAL1
PGE1
PTFT1
DA
PAL2
PGE2
PTFT2
CVL
SCVL2
SCVL1
CP
CAL1
CGE1
CTFT1
CA
NDA
CAL2
CGE2
CTFT2
HR
SP
SA

FIG. 4

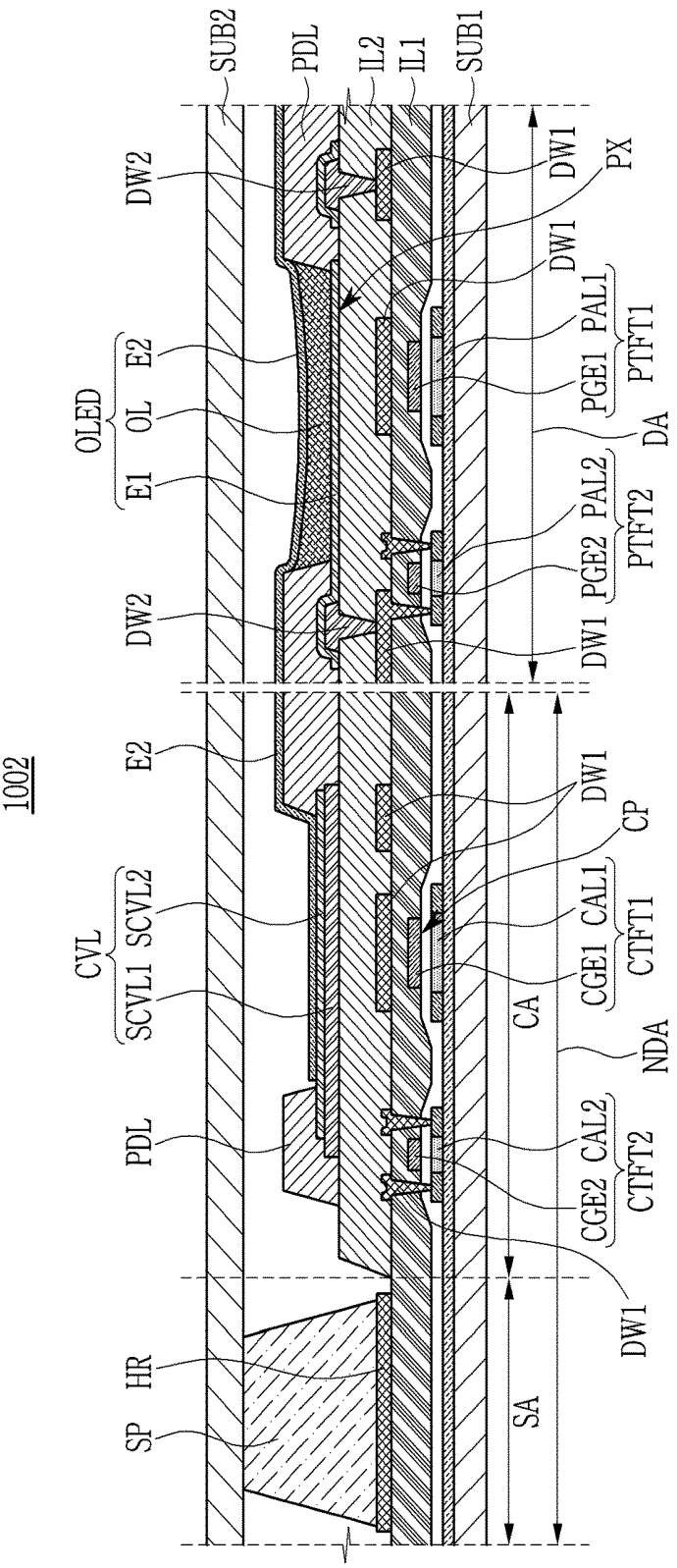
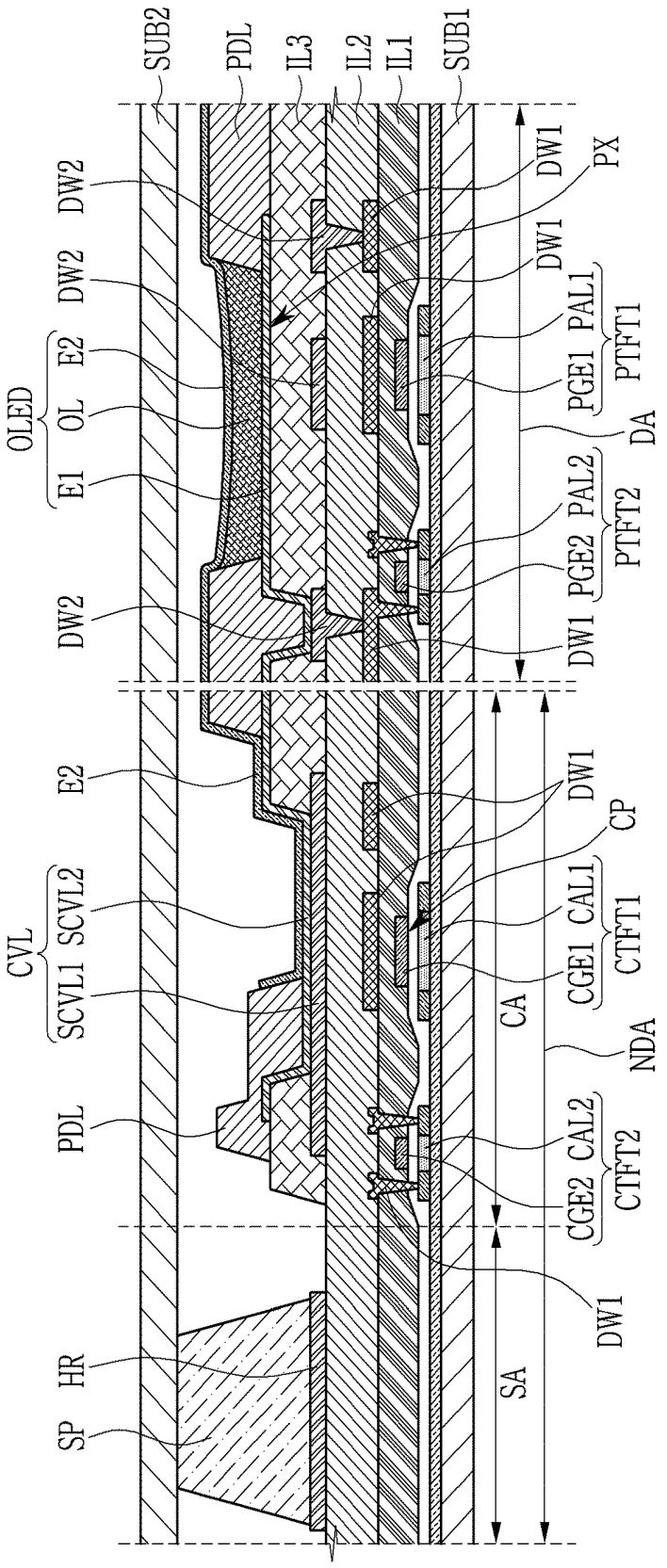

1002
SUB2
PDL
IL2
IL1
SUB1
DW2
DW1
PX
OLED
E2
OL
E1
PAL1
PGE1
PTFT1
DA
PAL2
PGE2
PTFT2
CVL
SCVL2
SCVL1
CP
CAL1
CGE1
CTFT1
CA
NDA
CAL2
CGE2
CTFT2
HR
SP
SA

FIG. 5


1003
SUB2
PDL
IL3
IL2
IL1
SUB1
DW2
DW2
OLED
E2
OL
E1
DW2
DW1
PX
DW1
PAL1
PGE1
PTFT1
DA
PAL2
PGE2
PTFT2
DW1
E2
CVL
SCVL2
SCVL1
PDL
DW1
CP
CAL1
CGE1
CTFT1
CA
NDA
CAL2
CGE2
CTFT2
DW1
SP
HR
SA

ORGANIC LIGHT EMITTING DIODE DISPLAY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2017-0161936, filed on Nov. 29, 2017 in the Korean Intellectual Property Office, the entire content of which is incorporated herein by reference.

BACKGROUND

1. Field

[0002] Aspects of embodiments of the present disclosure relate to an organic light emitting diode display.

2. Description of the Related Art

[0003] Generally, as examples of display devices, there are an organic light emitting diode (OLED) display, a liquid crystal display (LCD), and a plasma display panel (PDP).

[0004] Among them, the organic light emitting diode display includes a thin film transistor and an organic light emitting element positioned at a display area of a substrate, and a circuit unit and a common power supply line positioned at a non-display area of the substrate.

[0005] The circuit unit of the non-display area is electrically connected to the thin film transistor of the display area, and the common power supply line of the non-display area is electrically connected to the organic light emitting element of the display area.

[0006] The above information disclosed in this Background section is provided for enhancement of understanding of the background of the invention and, therefore, it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY

[0007] According to an aspect of exemplary embodiments, in an organic light emitting diode display, a width of a non-display area is minimized or reduced.

[0008] According to an aspect of exemplary embodiments, in an organic light emitting diode display, internal contamination may be suppressed.

[0009] According to one or more embodiments, an organic light emitting diode display includes: a substrate including a display area and a non-display area adjacent to the display area; a pixel thin film transistor positioned in the display area of the substrate; a first data wire positioned on the pixel thin film transistor; a second data wire positioned on the first data wire; an organic light emitting element positioned on the second data wire and electrically connected to the pixel thin film transistor through the first data wire and the second data wire; a circuit unit positioned in the non-display area of the substrate and including a circuit thin film transistor electrically connected to the pixel thin film transistor; and a common power supply line overlapping at least part of the circuit unit, electrically connected to the organic light emitting element, and formed on a same layer as the second data wire.

[0010] The non-display area may include: a circuit area adjacent to the display area, and including the circuit unit and the common power supply line; and a sealing area adjacent to the circuit area, and the organic light emitting diode display may further include a sealing part positioned in the sealing area.

[0011] The organic light emitting diode display may further include a heat reflection part in contact with the sealing part between the sealing part and the substrate.

[0012] The heat reflection part may not be in contact with the common power supply line or the circuit unit.

[0013] The heat reflection part may be positioned on the same layer as the second data wire.

[0014] The heat reflection part may be formed on a same layer as the first data wire.

[0015] The heat reflection part may include a same material as the second data wire.

[0016] The heat reflection part may include a same material as the first data wire.

[0017] The pixel thin film transistor may include a pixel active layer positioned on the substrate and a pixel gate electrode positioned on the pixel active layer, and the circuit thin film transistor may include a circuit active layer formed on a same layer as the pixel active layer and a circuit gate electrode formed on a same layer as the pixel gate electrode.

[0018] The organic light emitting diode display may further include a first insulating layer positioned between the pixel thin film transistor and the first data wire.

[0019] The organic light emitting diode display may further include a second insulating layer positioned between the first data wire and the second data wire.

[0020] The common power supply line may be positioned on the second insulating layer, and the circuit unit may be covered by the second insulating layer.

[0021] The organic light emitting element may include: a first electrode positioned on the second insulating layer; an organic emission layer positioned on the first electrode; and a second electrode positioned on the organic emission layer.

[0022] The common power supply line may include a first sub-common power supply line formed on the same layer as the second data wire, and a second sub-common power supply line in contact with the first sub-common power supply line and formed on a same layer as the first electrode.

[0023] The common power supply line may be in direct contact with the second electrode.

[0024] The first electrode and the second data wire may be in contact with the second insulating layer.

[0025] The organic light emitting diode display may further include a third insulating layer positioned between the second data wire and the first electrode.

[0026] The common power supply line may include a same material as the second data wire.

[0027] The common power supply line is formed by a same process as the second data wire.

[0028] According to an aspect of exemplary embodiments, an organic light emitting diode display with a minimized or reduced width of a non-display area is provided.

[0029] According to another aspect of exemplary embodiments, an organic light emitting diode display with suppressed internal contamination is provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIG. **1** is a top plan view showing an organic light emitting diode display according to an exemplary embodiment.

[0031] FIG. **2** is a circuit diagram showing a pixel shown in FIG. **1**.

[0032] FIG. **3** is a cross-sectional view taken along the line III-III of FIG. **1**.

[0033] FIG. **4** is a cross-sectional view of an organic light emitting diode display according to another exemplary embodiment, taken along a line corresponding to the line III-III of FIG. **1**.

[0034] FIG. **5** is a cross-sectional view of an organic light emitting diode display according to another exemplary embodiment, taken along a line corresponding to the line III-III of FIG. **1**.

[0035]

DESCRIPTION OF SYMBOLS

PTFT1: first pixel thin film transistor	DW1: first data wire
DW2: second data wire	OLED: organic light emitting element
CTFT1: first circuit thin film transistor	CP: circuit unit
CVL: common power supply line	

DETAILED DESCRIPTION

[0036] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which some exemplary embodiments of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

[0037] In order to more clearly explain the present invention, portions that are not directly related to the present invention may be omitted, and the same reference numerals are used in connection with the same or similar constituent elements throughout the specification.

[0038] In addition, the size and thickness of each configuration shown in the drawings may be arbitrarily shown for better understanding and ease of description, but the present invention is not limited thereto. In the drawings, the thicknesses of layers, films, panels, regions, etc., may be exaggerated for clarity. In the drawings, for better understanding and ease of description, the thicknesses of some layers and areas may be exaggerated.

[0039] It is to be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it may be directly on the other element or one or more intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Further, in the specification, the words "on" or "above" mean positioned on or below the object portion, and do not necessarily mean positioned on the upper side of the object portion based on a gravitational direction.

[0040] In addition, unless explicitly described to the contrary, the word "comprise" and variations such as "comprises" or "comprising" will be understood to imply the inclusion of stated elements, but not the exclusion of any other elements.

[0041] Next, an organic light emitting diode display according to an exemplary embodiment will be described with reference to FIG. **1** to FIG. **3**.

[0042] FIG. **1** is a top plan view showing an organic light emitting diode display according to an exemplary embodiment.

[0043] Referring to FIG. **1**, an organic light emitting diode display **1000** according to an exemplary embodiment includes a first substrate SUB**1**, a second substrate SUB**2**, a pixel Px, a circuit unit CP, a common power supply line CVL, a sealing part SP, and a driving unit DD.

[0044] In an embodiment, the first substrate SUB**1** and the second substrate SUB**2** include at least one among glass, quartz, ceramic, sapphire, plastic, etc. The first substrate SUB**1** and the second substrate SUB**2** may be rigid, flexible, stretchable, rollable, or foldable.

[0045] The first substrate SUB**1** includes a display area DA for displaying an image and a non-display area NDA neighboring the display area DA. In an embodiment, the non-display area NDA encloses the display area DA; however, the present invention is not limited thereto.

[0046] The non-display area NDA includes a circuit area CA to which the display area DA is adjacent and in which the circuit unit CP and the common power supply line CVL are positioned, and a sealing area SA in which the sealing part SP is positioned is adjacent to the circuit area CA. The circuit area CA is positioned between the display area DA and the sealing area SA.

[0047] The pixel Px is positioned in the display area DA of the first substrate SUB**1**. The pixel Px may be a minimum unit displaying an image. The pixel Px is electrically connected to the circuit unit CP, the driving unit DD, and the common power supply line CVL. The pixel Px may display the image by receiving a scan signal from the circuit unit CP, a data signal from the driving unit DD, and a common power supply from the common power supply line CVL.

[0048] In an embodiment, the pixel Px is electrically connected to a driving power supply line ELVDDL, thereby further receiving a driving power supply from the driving power supply line ELVDDL. For example, the driving power supply line ELVDDL may be positioned in at least one of the display area DA and the non-display area NDA of the first substrate SUB**1**.

[0049] FIG. **2** is a circuit diagram showing a pixel of FIG. **1**.

[0050] Referring to FIG. **2**, the pixel Px includes a plurality of pixel thin film transistors T**1**, T**2**, T**3**, T**4**, T**5**, T**6**, and T**7**, a plurality of wires Sn, S(n−1), S(n−2), EM, Vin, DAT, and ELVDDL that are selectively electrically connected to the plurality of pixel thin film transistors T**1**, T**2**, T**3**, T**4**, T**5**, T**6**, and T**7**, as well as a pixel capacitor Cst and an organic light emitting element OLED.

[0051] The plurality of pixel thin film transistors T**1**, T**2**, T**3**, T**4**, T**5**, T**6**, and T**7** includes a first thin film transistor T**1**, a second thin film transistor T**2**, a third thin film transistor T**3**, a fourth thin film transistor T**4**, a fifth thin film transistor T**5**, a sixth thin film transistor T**6**, and a seventh thin film transistor T**7**.

[0052] A first gate electrode G**1** of the first thin film transistor T**1** is respectively electrically connected to a third drain electrode D**3** of the third thin film transistor T**3** and a fourth drain electrode D**4** of the fourth thin film transistor T**4**, a first source electrode S**1** thereof is respectively electrically connected to a second drain electrode D**2** of the second thin film transistor T**2** and a fifth drain electrode D**5** of the fifth thin film transistor T**5**, and a first drain electrode D**1** thereof is respectively electrically connected to a third

source electrode S3 of the third thin film transistor T3 and a sixth source electrode S6 of the sixth thin film transistor T6.

[0053] A second gate electrode G2 of the second thin film transistor T2 is electrically connected to a first scan line Sn, a second source electrode S2 thereof is electrically connected to a data line DAT, and a second drain electrode D2 thereof is electrically connected to the first source electrode S1 of the first thin film transistor T1.

[0054] A third gate electrode G3 of the third thin film transistor T3 is electrically connected to the first scan line Sn, a third source electrode S3 thereof is electrically connected to the first drain electrode D1 of the first thin film transistor T1, and a third drain electrode D3 thereof is electrically connected to the first gate electrode G1 of the first thin film transistor T1.

[0055] A fourth gate electrode G4 of the fourth thin film transistor T4 is electrically connected to a second scan line S(n−1), a fourth source electrode S4 thereof is electrically connected to an initialization power supply line Vin, and a fourth drain electrode D4 thereof is electrically connected to the first gate electrode G1 of the first thin film transistor T1.

[0056] A fifth gate electrode G5 of the fifth thin film transistor T5 is electrically connected to a emission control line EM, a fifth source electrode S5 thereof is electrically connected to the driving power supply line ELVDDL, and a fifth drain electrode D5 thereof is electrically connected to the first source electrode S1 of the first thin film transistor T1.

[0057] A sixth gate electrode G6 of the sixth thin film transistor T6 is electrically connected to the emission control line EM, a sixth source electrode S6 thereof is electrically connected to the first drain electrode D1 of the first thin film transistor T1, and a first drain electrode D6 thereof is electrically connected to a seventh source electrode S7 of the seventh thin film transistor T7.

[0058] A seventh gate electrode G7 of the seventh thin film transistor T7 is electrically connected to a third scan line S(n−2), the seventh source electrode S7 thereof is electrically connected to the organic light emitting element OLED, and a seventh drain electrode D7 thereof is electrically connected to the fourth source electrode S4 of the fourth thin film transistor T4.

[0059] The plurality of wires includes the first scan line Sn transmitting a first scan signal to each of the second gate electrode G2 of the second thin film transistor T2 and the third gate electrode G3 of the third thin film transistor T3, the second scan line S(n−1) transmitting a second scan signal to the fourth gate electrode G4 of the fourth thin film transistor T4, the third scan line S(n−2) transmitting a third scan signal to the seventh gate electrode G7 of the seventh thin film transistor T7, the emission control line EM transmitting an emission control signal to each of the fifth gate electrode G5 of the fifth thin film transistor T5 and the sixth gate electrode G6 of the sixth thin film transistor T6, the data line DAT transmitting a data signal to the second source electrode S2 of the second thin film transistor T2, the driving power supply line ELVDDL supplying the driving power supply to each of one electrode of the pixel capacitor Cst and the fifth source electrode S5 of the fifth thin film transistor T5, and the initialization power supply line Vin supplying an initialization signal to the fourth source electrode S4 of the fourth thin film transistor T4.

[0060] The pixel capacitor Cst includes one electrode electrically connected to the driving power supply line ELVDDL and the other electrode that is electrically connected to each of the first gate electrode G1 of the first thin film transistor T1 and the third drain electrode D3 of the third thin film transistor T3.

[0061] The organic light emitting element OLED includes a first electrode, a second electrode positioned on the first electrode, and an organic emission layer positioned between the first electrode and the second electrode. The first electrode of the organic light emitting element OLED is respectively electrically connected to each of the seventh source electrode S7 of the seventh thin film transistor T7 and the sixth drain electrode D6 of the sixth thin film transistor T6, and the second electrode is electrically connected to the common power supply line CVL to which the common power supply is supplied.

[0062] The first scan line Sn, the second scan line S(n−1), the third scan line S(n−2), the emission control line EM, and the initialization power supply line Vin may be electrically connected to the circuit unit CP shown in FIG. **1**. The data line DAT may be electrically connected to the driving unit DD shown in FIG. **1**. The driving power supply line ELVDDL and the common power supply line CVL may be electrically connected to a terminal that is electrically connected to an external printed circuit board (PCB).

[0063] The pixel Px of the organic light emitting diode display **1000** according to an exemplary embodiment is configured of the plurality of pixel thin film transistors including the first thin film transistor T1 to the seventh thin film transistor T7, the pixel capacitor Cst, the first scan line Sn to the third scan line S(n−2), the data line DAT, the driving power supply line ELVDDL, and the initialization power supply line Vin; however, the present invention is not limited thereto, and the pixel of the organic light emitting diode display according to another exemplary embodiment may be configured of at least two pixel thin film transistors, at least one pixel capacitor, and wires including at least one scan line and at least one driving power supply line.

[0064] Referring to FIG. **1**, the circuit unit CP is positioned in the circuit area CA of the non-display area NDA of the first substrate SUB**1**. In an embodiment, the circuit unit CP includes two circuit units CP separated from each other by the display area DA of the first substrate SUB**1**; however, the present invention is not limited thereto, and one circuit unit CP or at least three circuit units CP may be included.

[0065] The circuit unit CP includes at least one circuit thin film transistor and at least one circuit capacitor. The circuit unit CP is electrically connected to the pixel Px. The circuit unit CP may be electrically connected to the first scan line Sn, the second scan line S(n−1), the third scan line S(n−2), the emission control line EM, and the initialization power supply line Vin of the pixel Px shown in FIG. **2**.

[0066] The common power supply line CVL is positioned on the circuit area CA of the non-display area NDA of the first substrate SUB**1**. The common power supply line CVL overlaps the circuit unit CP. The common power supply line CVL is positioned on the circuit unit CP. The common power supply line CVL is electrically connected to the second electrode of the organic light emitting element of the pixel Px.

[0067] The sealing part SP is positioned in the sealing area SA of the non-display area NDA of the first substrate SUB**1**. The sealing part SP encloses the display area DA of the first

substrate SUB1. The sealing part SP is positioned between the first substrate SUB1 and the second substrate SUB2 and adheres the first substrate SUB1 and the second substrate SUB2. In an embodiment, the sealing part SP includes a frit; however, the present invention is not limited thereto, and various organic materials or inorganic materials capable of adhering the first substrate SUB1 and the second substrate SUB2 may be included.

[0068] The driving unit DD is positioned in the non-display area NDA of the first substrate SUB1. In an embodiment, the driving unit DD may be an integrated circuit chip (IC chip) connected to the first substrate SUB1; however, the present invention is not limited thereto. The driving unit DD may be electrically connected to the data line DAT of the pixel Px shown in FIG. **2**.

[0069] Next, a stacking order of the organic light emitting diode display **1000** according to an exemplary embodiment will be described with reference to FIG. **3**.

[0070] FIG. **3** is a cross-sectional view taken along the line III-III of FIG. **1**.

[0071] Referring to FIG. **3**, the organic light emitting diode display **1000** according to an exemplary embodiment includes the first substrate SUB1, the second substrate SUB2, the pixel Px, a first insulating layer IL1, a second insulating layer IL2, a pixel definition layer PDL, the circuit unit CP, the common power supply line CVL, the sealing part SP, and a heat reflection part HR.

[0072] The first substrate SUB1 includes the display area DA, and the non-display area NDA including the circuit area CA and the sealing area SA. The pixel Px, the circuit unit CP, the common power supply line CVL, the sealing part SP, and the heat reflection part HR are positioned between the first substrate SUB1 and the second substrate SUB2.

[0073] The pixel Px is positioned in the display area DA of the first substrate SUB1, and includes a first pixel thin film transistor PTFT1, a second pixel thin film transistor PTFT2, a first data wire DW1, a second data wire DW2, and the organic light emitting element OLED.

[0074] The first pixel thin film transistor PTFT1 is positioned in the display area DA of the first substrate SUB1. The first pixel thin film transistor PTFT1 includes a first pixel active layer PAL1 positioned on a first substrate SUB1 and a first pixel gate electrode PGE1 positioned on the first pixel active layer PAL1. The first pixel active layer PAL1 includes a channel region overlapping with the first pixel gate electrode PGE1, and a source electrode and a drain electrode that do not overlap with the first pixel gate electrode PGE1.

[0075] The second pixel thin film transistor PTFT2 is positioned in the display area DA of the first substrate SUB1. The second pixel thin film transistor PTFT2 includes a second pixel active layer PAL2 positioned on the first substrate SUB1 and a second pixel gate electrode PGE2 positioned on the second pixel active layer PAL2. The second pixel active layer PAL2 includes a channel region overlapping with the second pixel gate electrode PGE2, and a source electrode and a drain electrode that do not overlap with the second pixel gate electrode PGE2.

[0076] Each of the first pixel thin film transistor PTFT1 and the second pixel thin film transistor PTFT2 may be one among the first thin film transistor T1 to the seventh thin film transistor T7 of the pixel Px shown in FIG. **2**.

[0077] The first data wire DW1 is positioned on the first pixel thin film transistor PTFT1 and the second pixel thin film transistor PTFT2. The first insulating layer IL1 is positioned between the first data wire DW1 and the first pixel thin film transistor PTFT1 and between the first data wire DW1 and the second pixel thin film transistor PTFT2.

[0078] The first data wire DW1 may include at least one line among the first scan line Sn of the pixel Px shown in FIG. **2**, the second scan line S(n−1), the third scan line S(n−2), the emission control line EM, the initialization power supply line Vin, the data line DAT, and the driving power supply line ELVDDL.

[0079] The second data wire DW2 is positioned on the first data wire DW1. The second insulating layer IL2 is positioned between the second data wire DW2 and the first data wire DW1.

[0080] The second data wire DW2 is in contact with the first data wire DW1 through a contact hole formed in the second insulating layer IL2. In an embodiment, the second data wire DW2 may include a different material from the first data wire DW1; however, the present invention is not limited thereto, and the same material as the first data wire DW1 may be included.

[0081] The second data wire DW2 may include at least one line among the first scan line Sn of the pixel Px shown in FIG. **2**, the second scan line S(n−1), the third scan line S(n−2), the emission control line EM, the initialization power supply line Vin, the data line DAT, and the driving power supply line ELVDDL.

[0082] The organic light emitting element OLED is positioned on the second data wire DW2 and is electrically connected to the second pixel thin film transistor PTFT2 through the first data wire DW1 and the second data wire DW2.

[0083] The organic light emitting element OLED includes a first electrode E1 positioned on the second insulating layer IL2, an organic emission layer OL positioned on the first electrode E1, and a second electrode E2 positioned on the organic emission layer OL.

[0084] At least one electrode of the first electrode E1 and the second electrode E2 may be one among a light transmitting electrode, a light reflective electrode, and a light translucent electrode. The light emitted from the organic emission layer OL may be emitted in at least one electrode direction of the first electrode E1 and the second electrode E2.

[0085] The first electrode E1 is electrically connected to the second pixel thin film transistor PTFT2 through the second data wire DW2 and the first data wire DW1.

[0086] The first electrode E1 and the second data wire DW2 are in contact with the second insulating layer IL2.

[0087] The first electrode E1 is partially exposed by the pixel definition layer PDL. An opening of the pixel definition layer PDL overlaps at least part of the first electrode E1.

[0088] The second electrode E2 extends from the display area DA to the non-display area NDA of the first substrate SUB1. The second electrode E2 is in direct contact with the common power supply line CVL in the non-display area NDA.

[0089] In an embodiment, a capping layer covering the organic light emitting element OLED may be positioned on the organic light emitting element OLED, and the second substrate SUB2 is positioned on the organic light emitting element OLED via the capping layer. In an embodiment, a thin film encapsulation layer may be positioned on the organic light emitting element OLED.

[0090] The first insulating layer IL1 is positioned between the first pixel gate electrode PGE1 and the first data wire DW1 of the first pixel thin film transistor PTFT1.

[0091] The second insulating layer IL2 is positioned between the first data wire DW1 and the second data wire DW2.

[0092] In an embodiment, the first insulating layer IL1 and the second insulating layer IL2 may include an inorganic insulating layer including at least one of a silicon nitride and a silicon oxide, or an organic insulating layer. The first insulating layer IL1 and the second insulating layer IL2 may be formed of a single layer or of multiple layers.

[0093] The pixel definition layer PDL may include the opening exposing at least part of the first electrode E1 of the organic light emitting element OLED, and may enclose the edge of the first electrode E1.

[0094] The circuit unit CP is positioned in the circuit area CA of the non-display area NDA of the first substrate SUB1, and includes a first circuit thin film transistor CTFT1, a second circuit thin film transistor CTFT2, and a first data wire DW1.

[0095] The first circuit thin film transistor CTFT1 is positioned in the circuit area CA of the first substrate SUB1. The first circuit thin film transistor CTFT1 includes a first circuit active layer CAL1 positioned on the first substrate SUB1 and a first circuit gate electrode CGE1 positioned on the first circuit active layer CAL1. The first circuit active layer CAL1 includes a channel region overlapping with the first circuit gate electrode CGE1, and a source electrode and a drain electrode that do not overlap with the first circuit gate electrode CGE1.

[0096] The second circuit thin film transistor CTFT2 is positioned in the circuit area CA of the first substrate SUB1. The second circuit thin film transistor CTFT2 includes a second circuit active layer CAL2 positioned on the first substrate SUB1 and a second circuit gate electrode CGE2 positioned on the second circuit active layer CAL2. The second circuit active layer CAL2 includes a channel region overlapping with the second circuit gate electrode CGE2, and a source electrode and a drain electrode that do not overlap with the second circuit gate electrode CGE2.

[0097] In an embodiment, the first circuit active layer CAL1 and the second circuit active layer CAL2 are formed on a same layer as the first pixel active layer PAL1 and the second pixel active layer PAL2. In an embodiment, the first circuit gate electrode CGE1 and the second circuit gate electrode CGE2 are formed on a same layer as the first pixel gate electrode PGE1 and the second pixel gate electrode PGE2.

[0098] The first circuit thin film transistor CTFT1 and the second circuit thin film transistor CTFT2 may be a part among the plurality of circuit thin film transistors included in the circuit unit CP. The first circuit thin film transistor CTFT1 and the second circuit thin film transistor CTFT2 are electrically connected to the first pixel thin film transistor PTFT1 and the second pixel thin film transistor PTFT2, which are positioned in the display area DA.

[0099] The first data wire DW1 is positioned on the first circuit thin film transistor CTFT1 and the second circuit thin film transistor CTFT2. The first insulating layer IL1 is positioned between the first data wire DW1 and the first circuit thin film transistor CTFT1 and between the first data wire DW1 and the second circuit thin film transistor CTFT2.

[0100] The plurality of circuit thin film transistors included in the circuit unit CP and the first data wire DW1 may have any of various disclosed circuit structures.

[0101] The common power supply line CVL is positioned on the circuit unit CP in the circuit area CA. The common power supply line CVL overlaps the circuit unit CP. The common power supply line CVL is electrically connected to the organic light emitting element OLED, and is in direct contact with the second electrode E2 of the organic light emitting element OLED.

[0102] In an embodiment, the common power supply line CVL is formed on a same layer as the second data wire DW2 positioned in the display area DA. In an embodiment, the common power supply line CVL includes a same material as the second data wire DW2. In an embodiment, the common power supply line CVL may be concurrently (e.g., simultaneously) formed with the second data wire DW2 by a process forming the second data wire DW2.

[0103] The second insulating layer IL2 is positioned between the common power supply line CVL and the first data wire DW1 of the circuit unit CP. The common power supply line CVL is positioned on the second insulating layer IL2, and the circuit unit CP is covered by the second insulating layer IL2.

[0104] In an embodiment, the common power supply line CVL includes a first sub-common power supply line SCVL1 and a second sub-common power supply line SCVL2.

[0105] In an embodiment, the first sub-common power supply line SCVL1 is formed on a same layer as the second data wire DW2 and includes a same material as the second data wire DW2.

[0106] The second sub-common power supply line SCVL2 is positioned on the first sub-common power supply line SCVL1 and is in direct contact with the first sub-common power supply line SCVL1. The second sub-common power supply line SCVL2 is positioned between the first sub-common power supply line SCVL1 and the second electrode E2 of the organic light emitting element OLED, and is in direct contact with the first sub-common power supply line SCVL1 and the second electrode E2. In an embodiment, the second sub-common power supply line SCVL2 may be formed on a same layer as the first electrode E1 of the organic light emitting element OLED, and may include a same material as the first electrode E1.

[0107] The sealing part SP is positioned in the sealing area SA of the non-display area NDA of the first substrate SUB1. The sealing part SP adheres the first substrate SUB1 and the second substrate SUB2, and is positioned between the first insulating layer IL1 and the second substrate SUB2. In an embodiment, the sealing part SP includes the frit, and is heated by a laser beam to adhere the first substrate SUB1 and the second substrate SUB2.

[0108] The heat reflection part HR is positioned between the sealing part SP and the first substrate SUB1. The heat reflection part HR is positioned between the first insulating layer IL1 and the sealing part SP, and is in direct contact with the sealing part SP and the first insulating layer IL1.

[0109] In an embodiment, the heat reflection part HR is formed on a same layer as the first data wire DW1 and includes a same material as the second data wire DW2. In an embodiment, the heat reflection part HR is concurrently (e.g., simultaneously) formed with the second data wire DW2 by a process forming the second data wire DW2.

[0110] The heat reflection part HR is not in contact with the common power supply line CVL or the circuit unit CP. In an embodiment, the heat reflection part HR has an island shape.

[0111] When heating the sealing part SP by using the heat of the laser beam, the heat reflection part HR again reflects the heat passing the sealing part SP toward the sealing part SP direction, thereby helping the sealing part SP to be easily heated.

[0112] As described above, in the organic light emitting diode display **1000** according to an exemplary embodiment, the common power supply line CVL is positioned on the same layer as the second data wire DW**2** to overlap the circuit unit CP on the circuit unit CP of the circuit area CA, thereof minimizing or reducing a plane width of the circuit area CA.

[0113] That is, the organic light emitting diode display **1000** with a minimized or reduced width of the non-display area NDA is provided.

[0114] Also, in the organic light emitting diode display **1000** according to an exemplary embodiment, the common power supply line CVL includes the first sub-common power supply line SCVL**1** positioned on the same layer as the second data wire DW**2** and the second sub-common power supply line SCVL**2** positioned on the same layer as the first electrode E**1**, thereby minimizing or reducing electrical resistance of the common power supply line CVL. Accordingly, the organic light emitting diode display **1000** suppressing the drop of the voltage of the common power supply passing through the second electrode E**2** from the common power supply line CVL due to the electrical resistance is provided.

[0115] Also, in the organic light emitting diode display **1000** according to an exemplary embodiment, as the heat reflection part HR in contact with the sealing part SP includes the same material as the second data wire DW**2** and is not in contact with the common power supply line CVL or the circuit unit CP, when heating the sealing part SP by using the heat of the laser beam, the heat passing the sealing part SP is suppressed from being transmitted to the common power supply line CVL and the circuit unit CP through the heat reflection part HR. As above-described, as the heat transmitted from the sealing part SP to the heat reflection part HR by the laser beam used during the manufacturing process is suppressed from being transmitted to the common power supply line CVL and the circuit unit CP, degradation of the first insulating layer IL**1**, the second insulating layer IL**2**, and the pixel definition layer PDL disposed in the non-display area NDA due to the heat is suppressed, and because the gas generated from the first insulating layer IL**1**, the second insulating layer IL**2**, and the pixel definition layer PDL is suppressed from being generated, the inside of the organic light emitting diode display **1000** is suppressed from being contaminated due to the gas.

[0116] That is, the organic light emitting diode display **1000** with suppressed internal contamination is provided,

[0117] As described above, the organic light emitting diode display **1000** with the minimized or reduced width of the non-display area NDA and also with the internal contamination being suppressed is provided.

[0118] Next, an organic light emitting diode display according to another exemplary embodiment will be described with reference to FIG. **4**.

[0119] Differences from the previously described organic light emitting diode display according to an exemplary embodiment will be described.

[0120] FIG. **4** is a cross-sectional view of an organic light emitting diode display according to another exemplary embodiment, taken along a line corresponding to the line III-III of FIG. **1**.

[0121] Referring to FIG. **4**, an organic light emitting diode display **1002** according to another exemplary embodiment includes the first substrate SUB**1**, the second substrate SUB**2**, the pixel Px, the first insulating layer IL**1**, the second insulating layer IL**2**, the pixel definition layer PDL, the circuit unit CP, the common power supply line CVL, the sealing part SP, and the heat reflection part HR.

[0122] The heat reflection part HR is positioned between the sealing part SP and the first substrate SUB**1**. The heat reflection part HR is positioned between the first insulating layer IL**1** and the sealing part SP, and is in direct contact with the sealing part SP and the first insulating layer IL**1**.

[0123] In an embodiment, the heat reflection part HR is formed on a same layer as the first data wire DW**1** and includes a same material as the first data wire DW**1**. In an embodiment, the heat reflection part HR is concurrently (e.g., simultaneously) formed with the first data wire DW**1** by a process forming the first data wire DW**1**.

[0124] The heat reflection part HR is not in contact with the common power supply line CVL or the circuit unit CP.

[0125] As described above, in the organic light emitting diode display **1002** according to another exemplary embodiment, the common power supply line CVL is positioned on the same layer as the second data wire DW**2** to overlap the circuit unit CP on the circuit unit CP of the circuit area CA, thereby minimizing or reducing the plane width of the circuit area CA.

[0126] That is, the organic light emitting diode display **1002** with the minimized or reduced width of the non-display area NDA is provided.

[0127] Also, in the organic light emitting diode display **1002** according to another exemplary embodiment, the common power supply line CVL includes the first sub-common power supply line SCVL**1** positioned on the same layer as the second data wire DW**2** and the second sub-common power supply line SCVL**2** positioned on the same layer as the first electrode E**1**, thereby minimizing or reducing the electrical resistance of the common power supply line CVL. Accordingly, the organic light emitting diode display **1002** in which the voltage of the common power supply passing the second electrode E**2** from the common power supply line CVL is suppressed from being dropped by the electrical resistance is provided.

[0128] Also, in the organic light emitting diode display **1002** according to another exemplary embodiment, as the heat reflection part HR in contact with the sealing part SP includes the same material as the first data wire DW**1** and is not in contact with the common power supply line CVL or the circuit unit CP, when heating the sealing part SP by using the heat of the laser beam, the heat passing the sealing part SP is suppressed from being transmitted to the common power supply line CVL and the circuit unit CP through the heat reflection part HR. As described above, as the heat transmitted from the sealing part SP to the heat reflection part HR by the laser beam used during the manufacturing process is suppressed from being transmitted to the common power supply line CVL and the circuit unit CP, the degra-

dation of the first insulating layer IL1, the second insulating layer IL2, and the pixel definition layer PDL disposed in the non-display area NDA due to the heat is suppressed, and because the gas generated from first insulating layer IL1, the second insulating layer IL2, and the pixel definition layer PDL is suppressed from being generated, the inside of the organic light emitting diode display **1002** is suppressed from being contaminated due to the gas.

[0129] That is, the organic light emitting diode display **1002** with suppressed internal contamination is provided.

[0130] As described above, the organic light emitting diode display **1002** with the minimized or reduced width of the non-display area NDA and also with the internal contamination being suppressed is provided.

[0131] Next, an organic light emitting diode display according to another exemplary embodiment will be described with reference to FIG. **5**.

[0132] Differences from the previously described organic light emitting diode display according to an exemplary embodiment will be described.

[0133] FIG. **5** is a cross-sectional view of an organic light emitting diode display according to another exemplary embodiment, taken along a line corresponding to the line III-III of FIG. **1**.

[0134] Referring to FIG. **5**, an organic light emitting diode display **1003** according to another exemplary embodiment includes the first substrate SUB1, the second substrate SUB2, the pixel Px, the first insulating layer IL1, the second insulating layer IL2, a third insulating layer IL3, the pixel definition layer PDL, the circuit unit CP, the common power supply line CVL, the sealing part SP, and the heat reflection part HR.

[0135] The third insulating layer IL3 is positioned between the second data wire DW2 and the first electrode E1 of the organic light emitting element OLED.

[0136] In an embodiment, the third insulating layer IL3 may include an inorganic insulating layer including at least one of a silicon nitride and a silicon oxide, or an organic insulating layer. The third insulating layer IL3 may be formed of a single layer or multiple layers.

[0137] The first electrode E1 of the organic light emitting element OLED is in contact with the second data wire DW2 through a contact hole formed in the third insulating layer IL3. The second data wire DW2 is in contact with the second insulating layer IL2, and the first electrode E1 is not in contact with the second insulating layer IL2.

[0138] In an embodiment, the common power supply line CVL includes the first sub-common power supply line SCVL1 and the second sub-common power supply line SCVL2.

[0139] In an embodiment, the first sub-common power supply line SCVL1 is positioned on the same layer as the second data wire DW2, and includes the same material as the second data wire DW2.

[0140] The second sub-common power supply line SCVL2 is positioned on the first sub-common power supply line SCVL1. The second sub-common power supply line SCVL2 is in direct contact with the first sub-common power supply line SCVL1 through the contact hole formed in the third insulating layer IL3.

[0141] The sealing part SP is positioned in the sealing area SA of the non-display area NDA of the first substrate SUB1. The sealing part SP adheres the first substrate SUB1 and the second substrate SUB2, and is positioned between the second insulating layer IL2 and the second substrate SUB2. In an embodiment, the sealing part SP includes the frit, and is heated by a laser beam to adhere the first substrate SUB1 and the second substrate SUB2.

[0142] The heat reflection part HR is positioned between the sealing part SP and the first substrate SUB1. The heat reflection part HR is positioned between the second insulating layer IL2 and the sealing part SP, and is in direct contact with the sealing part SP and the second insulating layer IL2.

[0143] In an embodiment, the heat reflection part HR is positioned on the same layer as the second data wire DW2 and includes the same material as the second data wire DW2. In an embodiment, the heat reflection part HR is concurrently (e.g., simultaneously) formed with the second data wire DW2 by a process forming the second data wire DW2.

[0144] The heat reflection part HR is not in contact with the common power supply line CVL or the circuit unit CP.

[0145] As described above, in the organic light emitting diode display **1003** according to another exemplary embodiment, the common power supply line CVL is positioned on the same layer as the second data wire DW2 to overlap the circuit unit CP on the circuit unit CP of the circuit area CA, thereby minimizing or reducing the plane width of the circuit area CA.

[0146] That is, the organic light emitting diode display **1003** with the minimized or reduced width of the non-display area NDA is provided.

[0147] Also, in the organic light emitting diode display **1003** according to an exemplary embodiment, the common power supply line CVL includes the first sub-common power supply line SCVL1 positioned on the same layer as the second data wire DW2 and the second sub-common power supply line SCVL2 positioned on the same layer as the first electrode E1, thereby minimizing or reducing electrical resistance of the common power supply line CVL. Accordingly, the organic light emitting diode display **1003** with the drop of the voltage of the common supply passing through the second electrode E2 from the common power supply line CVL due to the electrical resistance being suppressed is provided.

[0148] Also, in the organic light emitting diode display **1003** according to another exemplary embodiment, the heat reflection part HR in contact with the sealing part SP includes the same material as the second data wire DW2 on the same layer as the second data wire DW2 and is not in contact with the common power supply line CVL or the circuit unit CP, and when heating the sealing part SP by using the heat of the laser beam, the heat passing the sealing part SP is suppressed from being transmitted to the common power supply line CVL and the circuit unit CP through the heat reflection part HR. As described above, as the heat transmitted from the sealing part SP to the heat reflection part HR by the laser beam used during the manufacturing process is suppressed from being transmitted to the common power supply line CVL and the circuit unit CP, degradation of the first insulating layer IL1, the second insulating layer IL2, and the pixel definition layer PDL disposed in the non-display area NDA due to the heat is suppressed, and because the gas generated from the first insulating layer IL1, the second insulating layer IL2, and the pixel definition layer PDL is suppressed from being generated, the inside of the

organic light emitting diode display **1003** is suppressed from being contaminated due to the gas.

[0149] That is, the organic light emitting diode display **1003** with the suppressed internal contamination is provided.

[0150] According to an aspect, as described above, the organic light emitting diode display **1003** with the minimized or reduced width of the non-display area NDA and also with the suppressed internal contamination is provided.

[0151] While the present invention has been described in connection with what are presently considered to be some practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. An organic light emitting diode display comprising:
- a substrate including a display area and a non-display area adjacent to the display area;
- a pixel thin film transistor positioned in the display area of the substrate;
- a first data wire positioned on the pixel thin film transistor;
- a second data wire positioned on the first data wire;
- an organic light emitting element positioned on the second data wire and electrically connected to the pixel thin film transistor through the first data wire and the second data wire;
- a circuit unit positioned in the non-display area of the substrate and including a circuit thin film transistor electrically connected to the pixel thin film transistor; and
- a common power supply line overlapping at least part of the circuit unit, electrically connected to the organic light emitting element, and formed on a same layer as the second data wire.

2. The organic light emitting diode display of claim **1**, wherein
- the non-display area includes:
- a circuit area adjacent to the display area and including the circuit unit and the common power supply line; and
- a sealing area adjacent to the circuit area, the organic light emitting diode display further comprising a sealing part positioned in the sealing area.

3. The organic light emitting diode display of claim **2**, further comprising a heat reflection part in contact with the sealing part between the sealing part and the substrate.

4. The organic light emitting diode display of claim **3**, wherein the heat reflection part is not in contact with the common power supply line or the circuit unit.

5. The organic light emitting diode display of claim **4**, wherein the heat reflection part is positioned on the same layer as the second data wire.

6. The organic light emitting diode display of claim **4**, wherein the heat reflection part is formed on a same layer as the first data wire.

7. The organic light emitting diode display of claim **6**, wherein the heat reflection part includes a same material as the second data wire.

8. The organic light emitting diode display of claim **6**, wherein the heat reflection part includes a same material as the first data wire.

9. The organic light emitting diode display of claim **1**, wherein
- the pixel thin film transistor includes:
- a pixel active layer positioned on the substrate; and
- a pixel gate electrode positioned on the pixel active layer, and
- the circuit thin film transistor includes:
- a circuit active layer formed on a same layer as the pixel active layer; and
- a circuit gate electrode formed on a same layer as the pixel gate electrode.

10. The organic light emitting diode display of claim **1**, further comprising a first insulating layer positioned between the pixel thin film transistor and the first data wire.

11. The organic light emitting diode display of claim **10**, further comprising a second insulating layer positioned between the first data wire and the second data wire.

12. The organic light emitting diode display of claim **11**, wherein
- the common power supply line is positioned on the second insulating layer, and
- the circuit unit is covered by the second insulating layer.

13. The organic light emitting diode display of claim **11**, wherein the organic light emitting element includes:
- a first electrode positioned on the second insulating layer;
- an organic emission layer positioned on the first electrode; and
- a second electrode positioned on the organic emission layer.

14. The organic light emitting diode display of claim **13**, wherein the common power supply line includes:
- a first sub-common power supply line formed on the same layer as the second data wire; and
- a second sub-common power supply line in contact with the first sub-common power supply line and formed on a same layer as the first electrode.

15. The organic light emitting diode display of claim **13**, wherein the common power supply line is in direct contact with the second electrode.

16. The organic light emitting diode display of claim **13**, wherein the first electrode and the second data wire are in contact with the second insulating layer.

17. The organic light emitting diode display of claim **13**, further comprising a third insulating layer positioned between the second data wire and the first electrode.

18. The organic light emitting diode display of claim **1**, wherein the common power supply line includes a same material as the second data wire.

19. The organic light emitting diode display of claim **18**, wherein the common power supply line is formed by a same process as the second data wire.

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专利名称(译)	有机发光二极管显示器		
公开(公告)号	US20190165084A1	公开(公告)日	2019-05-30
申请号	US16/171162	申请日	2018-10-25
[标]申请(专利权)人(译)	三星显示有限公司		
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IPC分类号	H01L27/32 H01L51/52		
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摘要(译)

一种有机发光二极管显示器，包括：基板，包括显示区域和与显示区域相邻的非显示区域;像素薄膜晶体管，位于基板的显示区域;位于像素薄膜晶体管上的第一数据线;第二数据线位于第一数据线上;有机发光元件，位于第二数据线上，并通过第一数据线和第二数据线电连接到像素薄膜晶体管;电路单元，位于基板的非显示区域中，并包括电连接到像素薄膜晶体管的电路薄膜晶体管;公共电源线与电路单元的至少一部分重叠，电连接到有机发光元件，并形成在与第二数据线相同的层上。